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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/089,907	07/09/2002	Xiaoning Nie	57265 (45107)	1262

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EXAMINER
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PAN, DANIEL H

ART UNIT	PAPER NUMBER
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2183

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/089,907	NIE, XIAONING	
	<b>Examiner</b>	<b>Art Unit</b>	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 20 April 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 13,14,17,18,20 and 25-30 is/are pending in the application.
- 4a) Of the above claim(s) 1-12,15,16,19 and 21-24 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 13,14,17,18,20 and 25-30 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

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1. Claims 1-12,15,16,19,21-24 have been canceled. Claims 13,14,17,18,20,25-30 remain for examination. Limitations of claim 13 is not the same as original limitations in claim 13. Amended claim 13 is rejected under a new ground. Alpert et al. (5,559,986) in view of newly found art Matter et al. (5,634,131) is used in order address the new combined limitation of claim 13. Alpert et al. (5,559,986) and Irwin et al. (5,841,771) were cited on the record.

2. Applicant's arguments with respect to claims 13,14,17,18,20,25-30 have been considered but are moot in view of the new ground(s) of rejection.

3. Claim 13 is not being rejected under "101" as non-statutory because examiner believes that the practical application is to deactivate the execution unit upon the condition on first execution unit (see claim 13, lines 1-3 from the bottom). However, examiner would like to suggest changes in the use of language, such "operable" and "is designed", in order to avoid possibly broader interpretation of the claim. Applicant is reminded that the focus is not on the final result which is useful, tangible, and concrete, but rather than the final result which is useful, tangible, and concrete. The "operable" and the "is designed" are not a final result which is useful, tangible, and concrete. Correction of language is suggested in next response.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 13, 14, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alpert et al. (5,559,986) in view of Matter et al. (5,634,131).

5. As to claim 13, 30, Alpert disclosed a processor system (see fig.2) including at least

a) a program memory (main memory) (see the prefetch of instructions from main memory in col.5, lines 24-33),

b) instruction reading means (prefetcher) for reading out the instruction from the memory (see the prefetch of instructions from main memory in col.5, lines 24-33),

c) instruction decoding means (decoder 202) for decoding the instructions (see decoder in col.5, lines 31-33),

d) a plurality of executing units (203)(204)(205) operable in parallel of various instructions (see parallel execution in col.5, lines 38-41, lines 62-63), and the instruction read out means (prefetcher) and the decoder jointly provided for all execution units (see the prefetch and decoding of the instructions to the execution units in col.5, lines 31-51).

6. Alpert did not specifically show temporarily deactivate the first executing unit if momentarily no instruction to be executed as claimed. However, Matter taught a system for temporarily deactivating a first executing unit [floating point unit] if momentarily no instruction to be executed (see the disabled clock of a floating point

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unit when no instruction was to be executed in col.7, lines 20-37) . It would have been obvious to one of ordinary skill in the art to use Matter in Albert for deactivating the first executing unit if momentarily no instruction to be executed as claimed because the use of Matter could provide the ability of Albert to adjust to specific condition of the processor, and therefore, minimize the power consumption of the execution unit, and because Albert also taught to reduce the power consumption of the memory array in a processor (col.3, lines 46-54), which was a suggestion for the need for disabling the execution unit, and in do in so , provided a motivation. Alpert is used as primary reference because it showed clearly the plurality of execution units in parallel (see parallel execution' in col.5, lines 38-41 , lines 62-63) while Mater is used for showing the disabled execution unit [floating point].

7. Alpert's second execution unit was also used for executing only special instructions (see the floating point instruction in execution unit [205]).

8. Alpert also included a first execution unit (203) from executing all possible instructions (integer instructions) and a second execution unit (205) for execute required by the execution units (see the data cache 206 in col.5, lines 48-53).

9. As to claim 14, Alpert also included a temporary storage for storing information only a few instructions (floating point instructions, see col.5, lines 37-50).

10. Claim 20 is e rejected under 35 U.S.C. 103(a) as being unpatentable over Alpert et al. (5,559,986) in view Matter et al. (5,634,131) as applied to claim 13 and further in view Irwin et al. (5,841,771).

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11. As to claim 20, neither Alpert nor Matter did not specifically show the payload data as claimed. However, Irwin included header and payload data (see the separate header bus and payload bus in fig.9), transmitter and I/O ports (see 01.22, 23, Table 1). It would have been obvious to one of ordinary skill in the art to use Irwin in Alpert for including the payload data as claimed because the use of Irwin could provide Albert the ability to transmit the data in a predetermined format, such as the header and the payload, thereby increasing the transmission integrity of the data packet, and it could be achieved by reconfiguring the payload data of Irwin into Albert with modified system parameters (e.g. the data width, data type) into Albert so that specific payload data could be recognized by Albert in order to enhance the processing of the data transfer at a given I/O port.

12. Claims 17, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Albert et al. (5,559,986) in view Matter et al. (5,634,131) as applied to claims 13,14 above. and further in view of Berg (4,196,470).

13. As to claim 17, neither Alpert nor Matter specifically showed the move instruction disclosed one instruction for move a data block as claimed. However, Berg transferring data block (e.g. see col.3, lines 38-46). It would have been obvious to one of ordinary skill in the art to use Berg in Albert for including move instruction as claims because the use of Berg could provide the control capability of Alpert to adapt to specific type of data transfer based on a predetermined instruction format, such as a

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move instruction, and therefore, increasing the adaptability of the execution unit of Alpert, and because Alpert did show an offset values for a data block to be transferred (see the byte boundary in col.10, lines 1-2), which was a suggestion of the need of using an instruction for moving data block, and it could be achieved by configuring the control parameters to the move instruction (e.g. the transfer instruction type, and the instruction width) into Alpert so that move instruction was implemented in Alpert to achieve the enhance control, in doing so, provided a motivation.

14. As to claim 18, Alpert also included a storage or loading address of a data block to be stored or loaded, the amount of data elements, an offset value for storage or reading out (see the detailed references of the data line and size in the data cache memory in col.6, lines 39-67, col.7, lines 1-24, see also col.8, lines 21-42, col.9, lines 8-3 the byte boundary for the offset value in col.10, lines 1-2).

15. Claim 25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alpert et al. (5,559,986) in view Matter et al. (5,634,131) as applied to claims 13 above. and further in view of in view Irwin et al. (5,841,771) .

16. Alpert did not specifically show his first bus was slower than the second bus as claimed . However, Irwin taught a data processing system having a first bus (header) (see the fifth octet of header occupied 2 times the interval of one octet in 01.24, lines 60-67) which was at a lower rate than the second bus (see the 4 octets per 25.7ns in col.25, lines 9-13, see also the separate header bus and payload bus in fig.9). It would have been obvious to one of ordinary skill in the art to use Irwin in Alpert for including

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the slower rate as claimed because the use of Irwing could provide the ability of Albert to adjust to different speed, and therefore, providing the capability to accept a predefined set of data flow, and one of ordinary skill in the art should be able to recognize the advantage of using variable rate as being disclosed by Irwing into Alpert in order to achieve the enhanced flexibility in speed, and in doing so, provided a motivation.

17. As to claim 26, Alpert also included first data bus and second data bus (see the input and output connections to the execution units in fig.2 ) .

18. As to claim 27, Alpert also included a temporary storage of a bit stream of data block (see the detailed references of the data size in the data cache memory in col.6, lines 39-67, col.7, lines 1-24, see also col.8, lines 21-42).

19. As to claims 28,29, Alpert also included a first execution unit (203) connected to first data bus and the the execution unit (205) connected to scnd data bus (see the input and output connections to the execution units in fig.2). Abert's first execution can also connected to the second data bus (see bus connection in fig.2).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not



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mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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## ***21 Century Strategic Plan***

DANIEL H. PAN  
PRIMARY EXAMINER  
05/04/2011